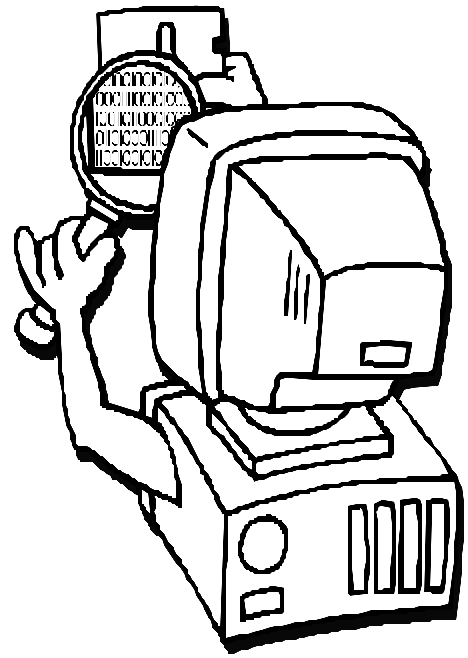
Complex Electronic Hardware

An Interactive Video Teletraining and Self-Study Course



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Federal Aviation Administration

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IVT Course Number 62816

Self-study Video course Number 25816

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How Do I Use This Guide?

This document is to be used for both the initial IVT broadcast and the self-study course. The guide provides you with the position of this course in the Systems Curriculum, an orientation to the IVT course, support materials for use during the broadcast and self-study, self-assessment and practice exercises, and both an IVT and self-study course evaluation.

Follow these steps to complete your study.

1. Read ***Section I, Systems Curriculum,*** to familiarize yourself with the the overall scope and format of the curriculum.
2. Review ***Section II, IVT Course Orientation***, before the broadcast, if possible, or before you watch the tape to get an overview of the purpose of the course, the target audience, the instructors, what you will learn, and the topics covered in the course.
3. Answer the pre-course self-assessment questions in ***Section III, Self-Assessment***.
4. Turn to ***Appendix A, Complex Electronic Hardware Presentation Visuals***, and refer to it during the broadcast or while watching the videotape. Appendix A contains the visual support material used by the instructors during the broadcast. You can use these visuals to take notes and follow along with the broadcast presentation. Begin the videotape here if you are completing this as a self-study course.
5. ***Appendices B through E*** contain materials to which the instructors will refer during the course.
6. Complete the post-course self-assessment in ***Section III, Self Assessment***.
7. Complete the appropriate form (IVT or self-study) in ***Appendix F***, ***Course Evaluation Forms***. For the IVT course, you will use the keypad you have been using during the course to complete the evaluation.

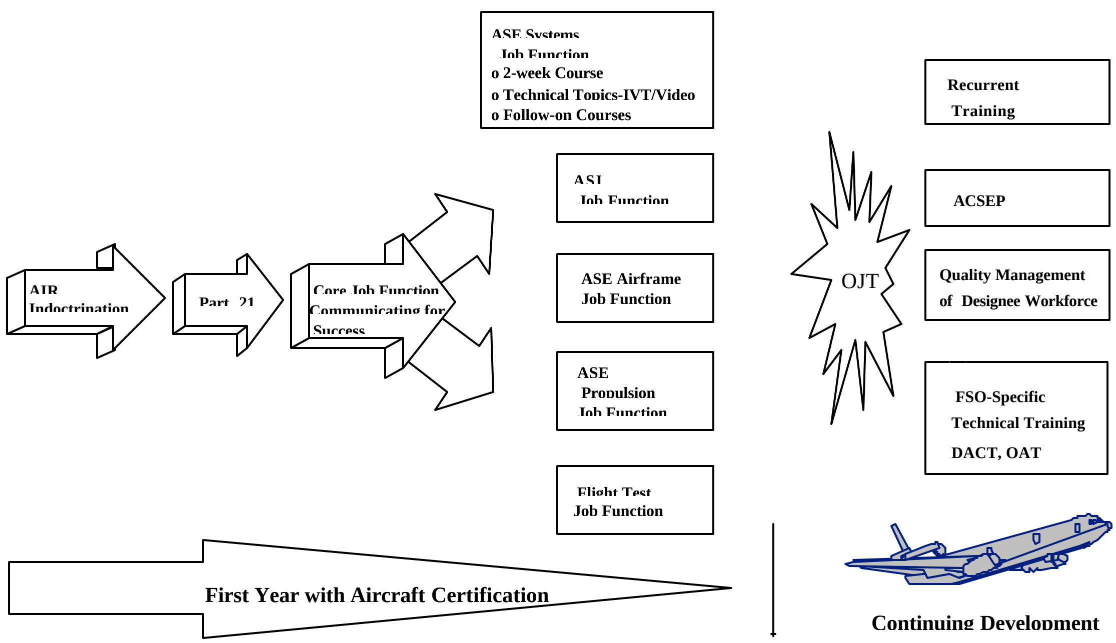
I. Systems Engineering Curriculum

What Does the Curriculum Cover?

The Systems Engineering Curriculum fits into the broader AIR Training Program that is summarized in the following figure.

The AIR Training Program

An Overview



Within the context of the AIR Training Program, the Systems Engineering Curriculum is designed to effectively meet the critical safety mission of the FAA by addressing the following Service goals:

Standardization

- Promote standardization throughout the organization in task accomplishment and application of airworthiness regulations in order to achieve uniform compliance.

Job Performance Proficiency

- Reduce significantly the time required for newly-hired engineers to attain full job performance proficiency.

Customer Service

- Establish and maintain appropriate, effective, and responsive communication, collaboration, leadership, and teamwork with both internal and external customers.

In addition to the Service goals, the Systems Engineering Curriculum is designed to provide ASEs with job function training in three domains:

- Tasks and procedures governing the work of engineers in design approval, technical project management, certificate management, and designee management.
- FAR airworthiness requirements that are the purview of electrical and mechanical systems engineers. Generally they are Subpart F of FAR parts 23, 25, 27, and 29.
- Technical subjects essential for all new engineers to meet both introductory requirements and, later, minimum technical proficiency level requirements.

The resulting Systems Engineering Curriculum structure consists of three main types of training opportunities —

1. Two-Week Job Function Course
2. Overviews of Technical Subjects
3. Follow-on Core Technical Subjects Courses

Two-Week Job Function Course

The Two-Week Job Function Course uses an instructor-led, classroom-based format with lecture, discussion, and individual and group activities. Supporting materials used in the course include print, overhead transparencies, videotapes, job aids, and documents and sample reports.

The course is divided into the following two major sections:

<u>*Section 1*</u>

- **Certification Tasks** — includes design approval, technical project management, certification management, and DER management.

<u>*Section 2*</u>

- **FAR Requirements and Key FAR Sections** — includes training in the subparts of the FAR that apply to electrical and mechanical systems engineers (Subpart F) at two levels: an overview of those subparts across FARs 23, 25, 27, and 29; and in-depth discussion of significant sections of the FAR that are important to the Service. The importance of these sections may stem from problems in interpretation and application of requirements, technical complexity of a design, "high visibility" projects, or safety considerations that are paramount.

Overviews of Technical Subjects

High-level overviews of 13 technical subjects are presented by NRSs, Technical Specialists or other senior engineers. These overviews are available in two modes:

- An initial live four-hour IVT satellite broadcast with accompanying course material is received at each Directorate and other downlink sites.
- A Video/Self-Study Training Package adapted from the initial IVT presentation is available through the Directorate Training Manager.

Basic concepts and FAA-specific applications and examples are provided for each of the following 14 technical subjects:

<u>For electrical engineers</u>

- Advanced Communications
- Advanced Display Systems/Heads-Up Displays

- Advanced Navigation
- Low Visibility/Autopilot

For mechanical engineers

- Crashworthiness and Interior Compliance
- Doors
- Icing

For both elecrical and mechanical engineers

- Automatic Flight Control Systems
- Complex Electronic Hardware
- HIRF and Lightning Protection
- Human Factors
- Software
- Systems Safety Analysis

Each technical subject overview is designed to not only provide ASEs with the FAA perspective on the topic, but also serve as an indicator of what further training may be needed.

Core Technical Subjects

As a follow-on to the Overviews of Technical Subjects, the curriculum will provide more in-depth training in the following two subject areas:

- System Safety Assessment
- Reliability & Probability

These core technical subjects are essential to the technical work of the systems engineer in a regulatory environment regardless of product or technology. Training in each of the core subjects will be designed to bring systems engineers to a minimum level of technical proficiency and to help promote proficiency in the application of the technical knowledge in an office work environment.

Additional technical training for engineers beyond these core subjects will depend largely on ACO organizational needs stemming from customer requirements, products certified, emerging technology, and the number of staff requiring more specialized training. In short, the more advanced the technical training required, the more individualized it becomes.

Such training topics could be as follows:

- HIRF
- Lightning
- Software Fundamentals
- Dynamic Seat Testing
- Icing Certification
- Accident Investigation
- Human Factors
- Flammability
- Interior Compliance & Crashworthiness

III. IVT Course Orientation

About This IVT Course

Complex Electronic Hardware (CEH) is one in a series of 13 "Overviews of Technical Topics" in the Systems Engineering Curriculum designed to prepare you to effectively meet the critical safety mission of the FAA. *[For more information on the Curricula, refer back to Section I of this guide.]*

Through a four-hour Interactive Video Teletraining (IVT) format, Leanna Rierson, the Software Program Manager for the FAA Aircraft Certification Service's Avionics Branch in Washington, D.C., Will Struck and Connie Beane, Aerospace Engineers with the Transport Airplane Directorate, will provide information to enhance your understanding of complex electronic hardware and its application in aviation.

What Is IVT?

Interactive Video Teletraining, or IVT, is instruction delivered using some form of live, interactive television. For the overview courses, the instructor delivers the course from the television studio at the FAA Academy in Oklahoma City. Through the IVT broadcast facility instructors are able to use a variety of visuals, objects, and media formats to support the instruction.

Participants are located at various receive sites around the country and can see the instructor and his/her materials on television sets in their classrooms. The participants can communicate with the instructor either through a microphone and/or the simple-to-use Viewer Response System Keypads. During the live presentation, when a participant has a question or the instructor asks for specific participant responses to questions, the participant(s) can signal to the instructor using their keypad. The collective participant responses or the name of a specific participant signalling a question are immediately visible to the instructor on the console at the broadcast site. The instructor can then respond as needed. When the instructor calls on a specific participant to speak from a site, participants calls on a specific participant to speak from a site, participants at each of the other sites can simultaneously hear the participant who is speaking.

This guide provides you with the framework for this course as well as the following appendices to be used for both the IVT and the self-study courses.

- Appendix A contains the actual visual support material used by the instructors during the broadcast. You can use these visuals to follow along with the videotape and record notes directly on the pages.
- Appendix B provides figures that will be referenced during the broadcast.
- Appendix C is a list of acronyms used in the course.
- Appendix D is a generic issue paper for part 25 airplanes.
- Appendix E lists a series of articles that will be used during the course and can serve as reference material back on the job.
- Appendix F provides the Course Evaluation Forms for the IVT broadcast and the self-study video course.

Who Is the Target Audience?

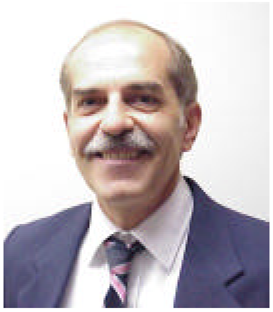
This course is designed for:

- Systems engineers who review and approve electronic and electrical systems containing complex electronic hardware for installation in aircraft
- Designated Engineering Representatives (DERs) and engineers in industry who are interested in the topic.

Who Are the Instructors?

Leanna Rierson

Leanna K. Rierson is the Software Program Manager for the FAA Aircraft Certification Service's Avionics branch in Washington, D.C. She has previous experience as a software engineer at NCR, Cessna Aircraft Company, and the Wichita Aircraft Certification Office. Leanna graduated suma cum laude, with a bachelor's degree in electrical engineering with emphasis in digital design. She is currently pursuing Master's and Ph.D. degrees in software engineering. Leanna is the leader for FAA's Software Grand Design program, Streamlining Software Aspects of Certification program, Flight Critical Systems Research effort, and Technical Router reUsable Software Team. She is also the chair of the international Certification Authorities Software Team and is the editorial leader of RTCA's Special Committee #190. At NCR, Leanna was involved in integrated circuit design and test; she has been involved in RTCA Special Committee #180 for the past 3 years.



Will Struck

Will Struck is currently working with the FAA Transport Airplane Directorate (TAD), Transport Standards Staff, Airplane and Flight Crew Interface Branch. He is responsible for TAD policy and guidance for software, programmable logic devices, electrical systems and equipment and Communication/Navigation/Surveillance systems. He has also been involved internationally in RTCA/EUROCAE joint committees and nationally in the FAA national software policy and notices. Will previously worked as a software DER and at Boeing and for the Department of Defense. Will has a Bachelor of Science Degree in Computer Science.

Connie Beane

Connie Beane is part of the Transport Airplane Directorate Standards Staff in Seattle, Washington. Her day-to-day responsibilities include Project Officer for the Atlanta and Chicago Aircraft Certification Offices. Connie has been with the FAA for 7 years and has worked in the Aviation Industry for 15 years. Since joining the FAA in 1992, she has been very active in the areas of software and electronic hardware policy and guidance efforts. Connie is the Federal representative and secretary for RTCA SC-180 which is currently developing design assurance guidelines for electronic airborne hardware. Connie has a BS in computer science from Ohio State University.

What Will You Learn?

After completing this course, you will be able to:

- Explain various types of complex electronic hardware (CEH)
- Describe current policy and practices of CEH
- Explain the current industry & government development of guidance
- Describe future FAA activities and plans.

What Topics Does the Course Cover?

The following topic outline is intended to give you an overview of the course content. In addition to this outline, Appendix A contains the visual presentation material used by the instructors during the broadcast.

I. Introduction
   - A. Introduction of Instructors (Connie, Leanna, Will)
   - B. Course Objectives (Leanna)
   - C. Course Outline (Leanna)

II. What is Complex Electronic Hardware? (Leanna)
   - A. Overview of Complex Electronic Hardware Technology
   - B. Applications Specific Integrated Circuits (ASICs)
   - C. Field Programmable Gate Arrays (FPGAs)
   - D. Other Programmable Logic Devices (PLDs)
   - E. Technology Trends
   - F. Summary

III. Use of Complex Electronic Hardware in Aviation (Will)
   - A. What's the Problem?
   - B. Generic Part 25 Issue Paper for Programmable Logic Devices
   - C. Current Practices
   - D. Certification Authority Expectations
   - E. Examples of Use in Aircraft
   - F. Summary

IV. Guidance Material Overview & Status (Connie)
   - A. RTCA SC-180/EUROCAE WG-46 History
   - B. Committee Charter
   - C. Difficulties Encountered
   - D. Document Overview
   - E. Current Document Status

F. Summary

V. Future FAA Activities (Leanna)
   A. Advisory Circular
   B. Designee Qualifications
   C. FAA Training
   D. Case Study

VI. Summary and Q/A (Connie, Leanna, Will)

III. Self-Assessment

Pre- & Post-Course Self-Assessment Questions

The instructors will ask you at the begining and end of the presentation to respond to the following four questions about complex electronic hardware.

Rate your confidence level for each of the following statements before and after completing the course.

1. I can explain the various types of complex electronic hardware.

	Very Confident	Moderately Confident	Not Confident
BEFORE THE COURSE:	☐	☐	☐
AFTER THE COURSE:	☐	☐	☐

2. I can describe the current policy and practices on complex electronic hardware.

	Very Confident	Moderately Confident	Not Confident
BEFORE THE COURSE:	☐	☐	☐
AFTER THE COURSE:	☐	☐	☐

3. I can explain the current industry and government development of guidance for complex electronic hardware.

	Very Confident	Moderately Confident	Not Confident
BEFORE THE COURSE:	☐	☐	☐
AFTER THE COURSE:	☐	☐	☐

4. I can describe the future FAA plans and activities in the area of complex electronic hardware.

	Very Confident	Moderately Confident	Not Confident
BEFORE THE COURSE:	☐	☐	☐
AFTER THE COURSE:	☐	☐	☐

Appendix A

Complex Electronic Hardware Presentation Visuals

Complex Electronic Hardware

Will Struck

Leanna Rierson

Connie Beane

IVT Hotline: (888) 279-8604

July 28, 1999 CEH-1

Instructors

- **Leanna Rierson**
  - **Phone: 202-267-3785**
  - **E-mail: Leanna.Rierson@faa.gov**
- **Will Struck**
  - **Phone: 425-227-2764**
  - **E-mail: Will.Struck@faa.gov**
- **Connie Beane**
  - **Phone: 425-227-2796**
  - **E-mail: Connie.Beane@faa.gov**

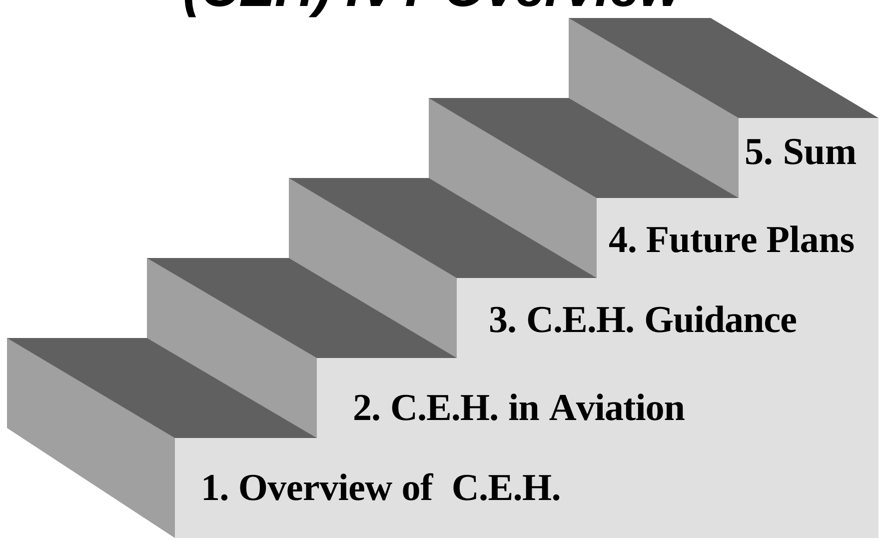
July 28, 1999 CEH-2

Course Objectives

- **Explain various kinds of complex electronic hardware**
- **Describe current policy & practices for complex electronic hardware**
- **Explain current industry/government development of guidance**
- **Describe future FAA activities & plans**

July 28, 1999 CEH-3

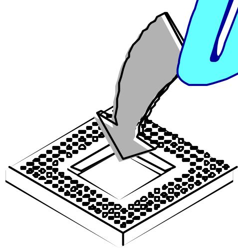
Complex Electronic Hardware (CEH) IVT Overview

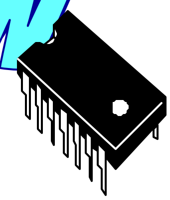


July 28, 1999 CEH-4

Complex Electronic Hardware

Overview





Leanna Rierson

FAA Aircraft Certification Service

Software Program Manager, Avionics

July 28, 1999 CEH-5

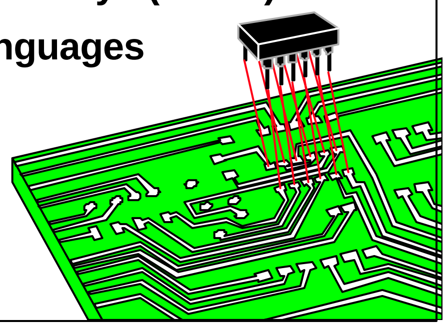
Section Objectives

- **Explain various kinds of complex electronic hardware (C.E.H.)**
  - **Describe common C.E.H. pitfalls**
  - **Describe what C.E.H. verification entails and why it is important**

July 28, 1999 CEH-6

Topics of Discussion

- Complex Electronic Hardware introduction
- Programmable logic devices (PLD)
- Application specific integrated circuits (ASIC)
- Field programmable gate arrays (FPGA)
- Hardware description languages
- Common C.E.H. pitfalls
- C.E.H. verification
- Summary



July 28, 1999

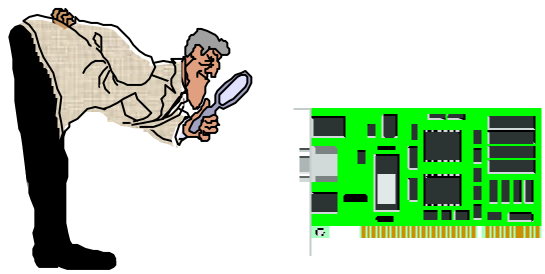
C.E.H. Introduction (1/3)

- Resources
  - FAA Handbook
    - »(DOT/FAA/AR-95/125-III, 2)
  - EDN
    - »(www.ednmag.com)
  - Computer design
    - »(www.computer-design.com)
  - Modular series on solid state devices
    - »Addison-Wesley
  - FPGA (by Oldfield & Dorf)

July 28, 1999 CEH-8

C.E.H. Introduction (2/3)

- **What is *COMPLEX*?**
  - **Not simple**
  - **Cannot be exhaustively tested**
  - **Cannot be 100% tested**



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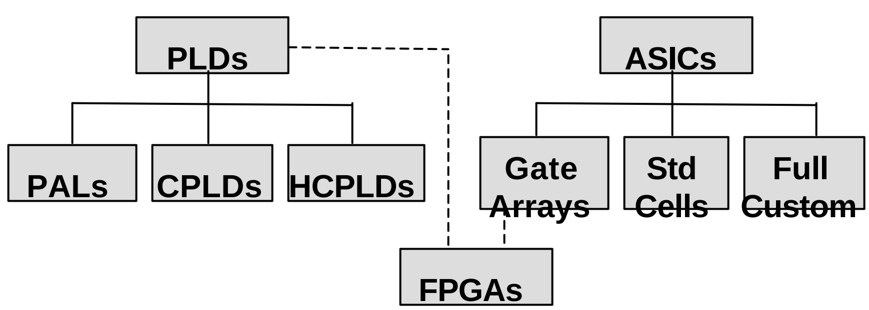
C.E.H. Introduction (3/3)

2 Major Categories



PLD = Programmable logic device **PAL = Programmable array logic** **CPLD = Complex PLD** **HCPLD = High-capacity PLD**	**ASIC = Application-specific integrated circuit** **FPGA = Field programmable gate array**

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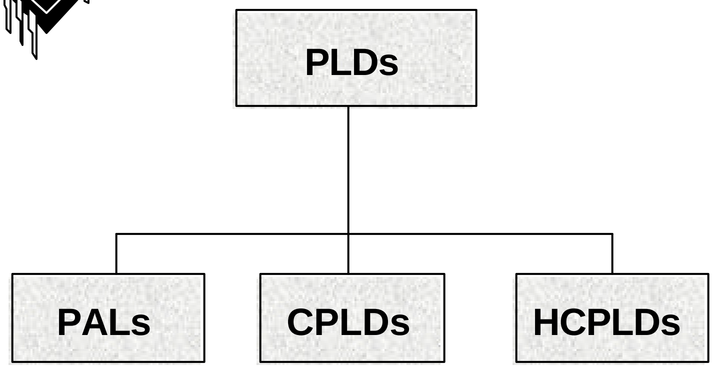
PLDs (1/4)



PLD = Programmable logic device
PAL = Programmable array logic
CPLD = Complex PLD
HCPLD = High-capacity PLD

July 28, 1999 CEH-11

PLDs (2/4)

- **Programmable array logic (PAL)**
  - **Reference Figures 1 & 2 of App B**
  - **Boolean logic elements**
    - » **AND, OR, NOT**
  - **Address decoders or small controllers**
  - **Least complex programmable logic**
  - **Called SPLD (simple PLD) by some sources**

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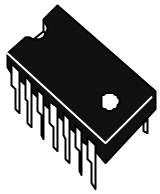
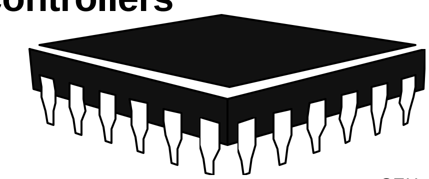


PLDs (3/4)

- **Complex PLDs (CPLDs)**
  - **Reference Figure 3 of App B**
  - **Many PLDs in a single device**
  - **Complex state machines**
  - **High-speed operation**
  - **Bus interface controllers**



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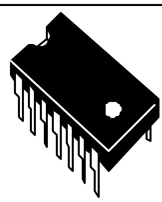

PLDs (4/4)

- **High-capacity PLDs (HCPLDs)**
  - **Even more gates than CPLDS**
  - **Some have 50,000 gates**
  - **Used to prototype gate arrays**
  - **Called CPLD by some sources**

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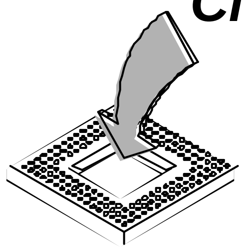
Application-Specific Integrated Circuit (ASICs) (1/3)



ASICs

- Gate Arrays
- Std Cells
- Full Custom

ASIC = Application-specific integrated circuit

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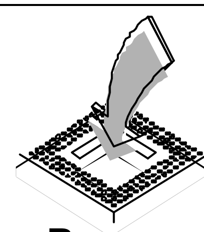
ASICs (2/3)



- **Gate array vs standard cell**
  - **Reference Figures 4 and 5 of App B**
  - **Logic blocks same for gate array**
  - **Logic blocks differ for standard cell**

Characteristic	Gate Array	Standard Cell
Nonrecurring Engr Cost	Low	High
Per Piece Cost	High	Low
Utilization	Low	High
Turnaround Time	Fast	Slow
Customizability	Low	High

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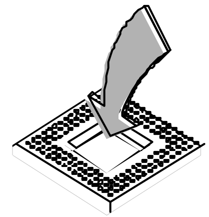
ASICs (3/3)



- **Full Custom**
  - **Logic blocks customized by designer**
  - **Most expensive**
  - **Full custom digital ICS**
  - **Full custom linear ICS**

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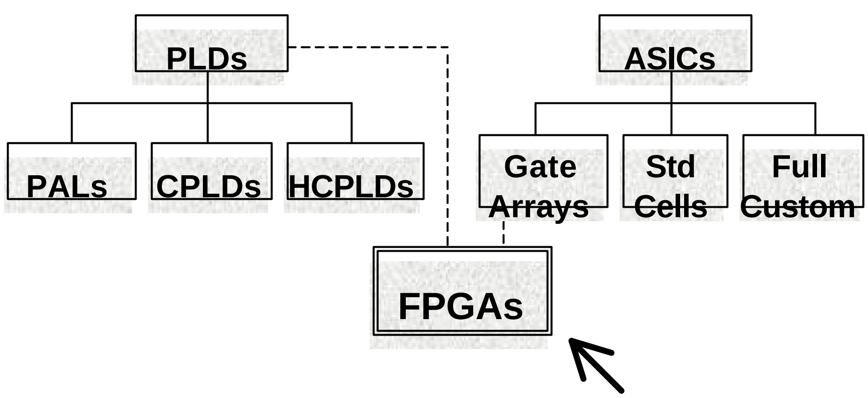
Field Programmable Gate Array (FPGAs) (1/4)



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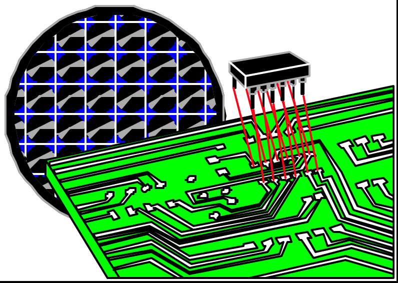
FPGAs (2/4)

- Customized
- Programmable logic device
- High density of gates
- Program internal connections
- Reference Figure 6 of Appendix B



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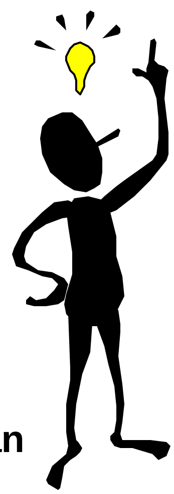
FPGAs (3/4)

- Advantages of FPGA
  - Reliability
  - Higher densities
  - Supported by hardware description languages (HDLS)
  - Architectural flexibility
  - Can be more cost effective than standard cell for low volumes



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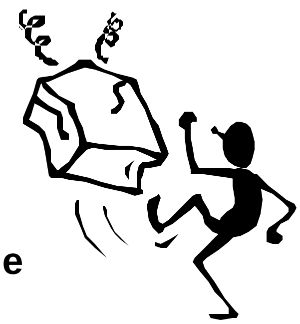
FPGAs (4/4)

- **Disadvantages of FPGA**
  - **Development cost is higher then PLDS**
  - **Not as easy to use as PLDS due to complexity**
  - **May require use of HDL to manage complexity**
  - **High unit cost**
  - **Timing difficult to handle**



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Hardware Description Language (HDL) (1/6)

- **Definition**
  - **Specialized programming language**
  - **Describes physical design, electronic behavior, logic structure, and system annotation information for circuits**
  - **Allows design description at a high level of abstraction**
  - **Supports a logical synthesis path to gate-level implementation**

(reference: FAA Handbook)

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HDL (2/6)

2 Dominant Languages

Verilog HDL

Very High Speed Integrate Circuit HDL (VHDL)

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HDL (3/6)

- **VHDL**
  - **Mandated by DOD in 1987**
  - **Intended to reduce production times & life cycles for digital systems procured by government**
  - **3 levels of construct abstraction:**
    - »**Structural**
    - »**Data flow**
    - »**Behavioral**

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HDL (4/6)

- **Verilog HDL**
  - **Most widely used HDL**
  - **Capabilities similar to VHDL**
  - **Considered to be easier to learn and use than VHDL**

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HDL (5/6)

- **Advantages of VHDL and Verilog HDL**
  - **Easier to make changes on computer**
  - **Isolate designer from constantly changing technology**
  - **Allow use of synthesis tools to complete design**
  - **Allow hardware and library reuse**
  - **Allow for standardization among vendors**

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HDL (6/6)

- Disadvantages of VHDL & Verilog HDL
  - Different versions of VHDL & Verilog HDL
  - Doesn't handle timing

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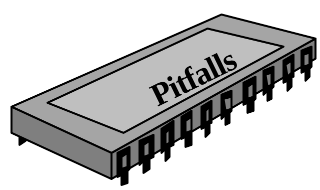
Common C.E.H. Pitfalls (1/3)

- Logic designs pitfalls
  - Clock-related errors
  - Race conditions



- Metastability
- Noise and ground practices
- Latch-up
- Single event upset

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Common C.E.H. Pitfalls (2/3)

- **Submicron technology issues**
  - **Gate delays**
  - **Floorplanning**
  - **Crosstalk**
  - **Power & thermal issues**
- **Software issues**

July 28, 1999 CEH-29

Common C.E.H. Pitfalls (3/3)

- **Packaging issues**
  - **I/O pin connections**
  - **Device mounting heat dissipation (millions of transistors on a chip)**
  - **Temperature sensitivity**
  - **Electronic discharge (ESD) protection**

July 28, 1999 CEH-30

C.E.H. Verification (1/2)

- **Traditional hardware verification**
  - **Exhaustive testing**
- **Traditional software verification**
  - **Emphasis on process**
  - **Requirements testing and structural coverage**

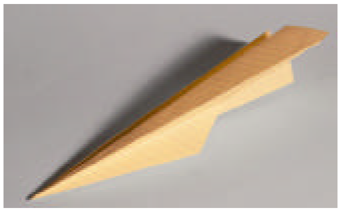
July 28, 1999 CEH-31

C.E.H. Verification (2/2)

- **C.E.H. verification**
  - **Cannot rely on process alone**
  - **Cannot perform pin-to-pin testing**
  - **Verification techniques commonly used**
    - »**Design for testability**
    - »**Test synthesis**
    - »**Still evolving**

July 28, 1999 CEH-32

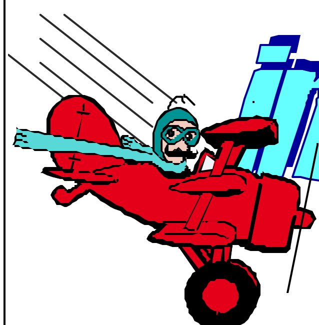
Summary



- C.E.H. here to stay
- PLDs, ASICs, and FPGAs
  most common C.E.H. used in aircraft
- Hardware description languages
  assist development of C.E.H.
- Many potential pitfalls in design and
  use of C.E.H.
- Verification as important as design

July 28, 1999 CEH-33

Complex Electronic Hardware in Aviation



Will Struck

FAA Transport Airplane Directorate

Transport Standards Staff, ANM-111

July 28, 1999 CEH-34

Section Objectives

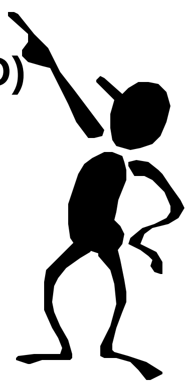
- Describe current policy and practices for C.E.H.
  - State current status associated with C.E.H. assurance used in airborne systems
  - Provide examples

Focus is part 25 aircraft

July 28, 1999 CEH-35

Topics of Discussion

- What's the concern ??
- Generic part 25 issue paper for programmed logic devices (PLD)
- Current practice
- FAA expectations
- Examples of aircraft uses
- Summary



July 28, 1999 CEH-36

What's the Concern ??

- Hardware or software?
- Simple or complex?
- Increasing complexity and parts reduction
- Obsolete parts replacement
- Hardware design assurance
- Inconsistent application

July 28, 1999 CEH-37

Hardware or Software (1/2)

- Digital computing or logic device
  - When is it hardware?
  - When is it software?
- Problem: No regulations or guidance address complex electronic hardware except in context of "system"

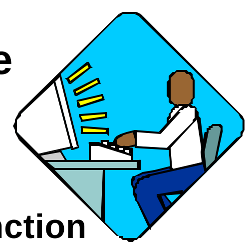
July 28, 1999 CEH-38

Hardware or Software (2/2)

- AC 20-115B and RTCA DO-178B address software design assurance
- AC 25.1309-1A "System Analysis and Design" addresses fail-safe design
- No guidance exists specifically for electronic hardware design assurance

July 28, 1999 CEH-39

Simple or Complex (1/2)

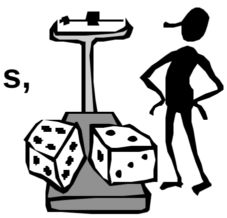


- Simple electronic hardware
  - Relatively easy to prove
    - »Intended function
    - »Contains no unintended function
  - Assumed it will perform only intended function until it wears out, breaks, or is affected by an external event

July 28, 1999 CEH-40

Simple or Complex (2/2)

- **Complex electronic hardware**
  - **Straightforward to prove intended function**
  - **Very hard or impossible to prove unintended function or malfunction because of complexity**
- **Answer: Hardware Design Assurance**
  - **Structured disciplined process commensurate with risk (hazards, failure conditions)**



July 28, 1999 CEH-41

Increasing Complexity

- **Not a big concern in past, most airborne hardware simple, verifiable**
- **Advances in electronics technology**
  - **Increased functionality (adding new functions and combining formerly separate functions)**
  - **Increased complexity (30K-250K gates/ logic points)**

July 28, 1999 CEH-42

Parts Reduction

- Aircraft systems developers embracing new technology for parts reduction, replacing obsolete parts
- Escape from RTCA DO-178B?

July 28, 1999 CEH-43

Obsolete Parts Replacement

- Becoming issue as
  - Older parts no longer being produced
  - Technology evolves
  - Fewer military-standard parts available

July 28, 1999 CEH-44

CAST Position Paper (P-32)

- CAST Position Paper being drafted
  - Perform change impact analysis of obsolete part replacement on software, other hardware, and system
  - Identify all impacted components and attributes and change significance
  - Coordinate with Certification Authorities
  - Re-verify and get approval

July 28, 1999 CEH-45

Hardware Design Assurance: Problem

- No correlation between design and device except reliance on tool
- Hard to prove no malfunction paths in device, no visibility into internal logic or its layout
- Must have qualification of tool, *adequate* test of device, comparison of test results with simulation results, etc.

July 28, 1999 CEH-46

Inconsistent Application

- Different ACO engineers and DERs apply different criteria for approval of C.E.H.
- Many engineers do not even address C.E.H. except in “system” context
- Lack of knowledge and guidance impacted certification program schedules and costs

July 28, 1999 CEH-47

Related Regulations

- FAR Part 23/25 Subpart F - Equipment
  - 23/25.1301, 23/25.1309 - be designed and perform intended function; also 33.28
  - No single failure or malfunction should result in a catastrophic or hazardous or major failure condition
  - Combinations of multiple failures or malfunctions (cascading or common cause) should be mitigated

July 28, 1999 CEH-48

Guidance - AC 23/25.1309-1C/1A/B

- **"System Design and Analysis" - "FAA Fail Safe Design Concept"**
  - ***In any system or subsystem, the failure of any single element, component, or connection … should be assumed regardless of its probability***
  - **Fail-safe design principles, including designed integrity, redundancy, isolation, proven reliability, failure effect limits, safety margins, ...**

July 28, 1999 CEH-49

Aircraft Safety and Design (1/2)

- **Aircraft Safety Assessment identifies hazards and failure conditions related to aircraft functions**
- **Aircraft Architecture - mitigates hazards using safety monitors, redundancy, dissimilar systems, backups, independence, limiters, etc.**

July 28, 1999 CEH-50

Aircraft Safety and Design (2/2)

- Aircraft Safety Assessment
  - Determines safety requirements and margins of aircraft functions
  - Evaluates systems' contribution to functions and potential hazards
  - Determines failure conditions and potential of systems to contribute to hazards

July 28, 1999 CEH-51

System Safety and Design (1/2)

- AC 23.1309-1C, 25.1309-1A/B
- SAE ARP 4754 and ARP 4761
- Other guidance - RTCA & SAE, Military Standards, EQT DO-160D, AC, FAA Orders and Notices, Issue Papers - HIRF, Lightning, EME/EMI, Displays, etc.

July 28, 1999 CEH-52

System Safety and Design (2/2)

- **Perform safety assessment at system level**
  - **Ensure reliability and integrity requirements of system can be met by hardware assembly/sub-assemblies/ components, including software and hardware components**
- **System may use redundancy, monitoring, etc. internally to address safety requirements**

July 28, 1999 CEH-53

Hardware Safety and Design

- **No government or industry standard**
- **RTCA SC-180 DO-TBD / EUROCAE WG-46 ED-80 in work past 6 years**
  - **Currently Draft 17+**
- **Issue Paper used for simple and complex programmable logic devices in lieu of industry standard**

July 28, 1999 CEH-54

Generic Part 25 PLD Issue Paper (1/3)

- **Requirements for simple device:**
  - **PLDs whose failure or malfunction could result in a catastrophic or hazardous failure condition for the aircraft shall undergo testing that demonstrates correct operation under all combinations and permutations of conditions of the gates within a device or analyses that can show analogous results**

July 28, 1999 CEH-55

Generic Part 25 PLD Issue Paper (2/3)

- **Requirements for simple device (cont.):**
  - **PLDs whose failure or malfunction could result in a major or minor failure condition for the aircraft shall undergo testing that demonstrates correct operation under all combinations and permutations of conditions at the pins of a device or analyses that can show analogous results**

July 28, 1999 CEH-56

Generic Part 25 PLD Issue Paper (3/3)

- For simple and complex - requirements and verification (test and/or analysis) documented, CM of data, quality control of manufacturing
  - If simple, test and/or analyze to appropriate level (gate or pin)
  - If complex (i.e., requirements technically infeasible because of device complexity), do rigorous, structured development commensurate with the risk and verify

July 28, 1999 CEH-57

Current Practice (1/2)

- Some airframers and their suppliers have internal guidance that they impose and/or apply for these devices
- Typical applicant response: Company guidance will be followed, except for those previously approved with no change and those of “minor” failure condition classification

July 28, 1999 CEH-58

Current Practice (2/2)

- Many companies do not have "defined" process for C.E.H. but are developing
- Some companies develop process using "folklore" method
- "Credit" usually allowed for devices already used in certified systems
- New and modified devices are focus of issue paper

July 28, 1999 CEH-59

Expectations (1/4)

- Safety assessment addresses both device failure (reliability, availability) and correct function (integrity)
- System architecture and strategies used to mitigate unacceptable risks
- System requirements, including safety requirements, allocated to hardware

July 28, 1999 CEH-60

Expectations (2/4)

- In certification plans, device identification, safety classification, function, and if new or previously approved for intended use
- If new, means of compliance and evidence of assurance
- If previously approved, service history and relevance to planned use

July 28, 1999 CEH-61

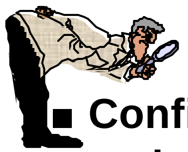
Expectations (3/4)

DATA

- Plans (dev., verif., CM and QA)
- Requirements
- Design & implementation data
- Tool qualification, if needed
- Verification & validation procedures
- V&V results

July 28, 1999 CEH-62

Expectations (4/4)



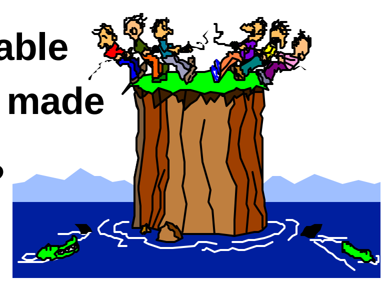
DATA

- Configuration and data management and control, CM records
- Quality assurance, control and records
- Installation/assembly data
- Acceptance test procedures
- Evidence of compliance summarized in Accomplishment Summary

July 28, 1999 CEH-63

Real Life

- Experience shows:
  - Both good and not so good examples
  - Misinterpretations, inconsistent application
  - ASIC tool support available
  - Overall, progress being made
- *Is enough being done?*
- *Is too much expected?*



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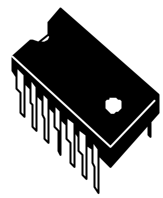
Aircraft Use Examples (1/2)

- "Glue" logic on hardware computing devices for interface to software
- Microprocessors and micro-coded instructions



- Memory management units
- Input/output devices - e.g., ARINC 429 ASIC
- Converters - Analog to digital (A/D) and digital to analog (D/A)

July 28, 1999 CEH-65

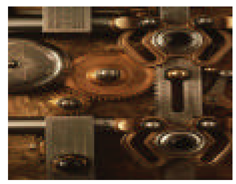
Aircraft Use Examples (2/2)

- Combined flight control functions
- Combined RA and TAWS functions
- Digital flight deck clock (replace analog plus added functionality)
- Large displays (primary, secondary, and multi-function)
- Independent company well-defined CEH process (will build/verify for a fee)

July 28, 1999 CEH-66

Summary

- Concerns about increasing complexity
- Additional guidance needed now
- Current approach is issue paper and internal company guidance
- Obsolete parts an issue - “must replace” parts & workload concerns
- Progress being made



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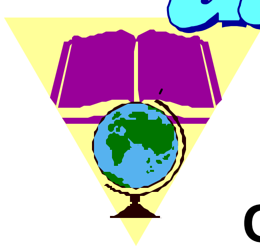
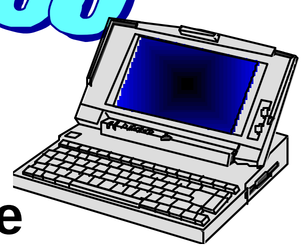
Complex Electronic Hardware Guidance





Connie Beane

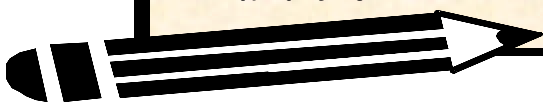
FAA Transport Airplane Directorate

Transport Standards Staff, ANM-113

July 28, 1999 CEH-68

Section Objectives

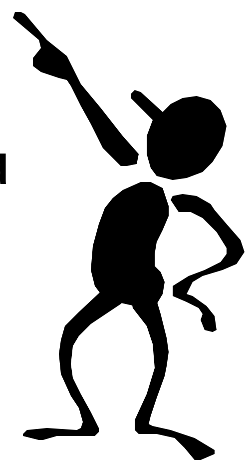
- Explain current industry/ government development of guidance
  - State current status of guidance being developed
  - Describe what the future looks like for applicants and the FAA



July 28, 1999 CEH-69

Topics of Discussion

- History of committee
- Committee charter
- Difficulties encountered
- Document content
- Methods to use
- Current status
- Summary



July 28, 1999 CEH-70

RTCA SC-180

- History
  - First meeting October 1993
  - First joint RTCA/EUROCAE meeting May 1994
  - Created to address design assurance for programmable logic devices (PLDS)
  - Expanded to include all electronic airborne hardware

July 28, 1999 CEH-71

SC-180 Charter

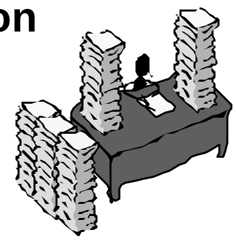
- To develop design assurance guidelines for electronic airborne hardware
- Flexible enough to allow use of emerging/state-of-the-art technology
- Guidelines applicable to devices built in-house and bought off-the-shelf
- Incorporate best practices of today's development environment

July 28, 1999 CEH-72

Difficulties Encountered (1/2)

- Defining *simple* versus *complex*
  - No agreed-to, industry-wide definition of *complex*
  - Debate within committee

- Industry fear of over-regulation
- Misinterpretation of whatever guidelines SC-180 developed



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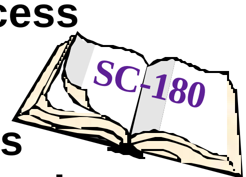
Difficulties Encountered (2/2)

- Off-the-shelf devices
  - Cheaper to buy than to build
  - Lack of stringent requirements for safety
  - Aerospace too small a market
  - Documentation unavailable or insufficient
- System engineering perspective prevalent

July 28, 1999 CEH-74

Document Content

- Structured similar to DO-178B, software considerations in airborne systems and equipment certification
- Covers hardware lifecycle process excluding manufacturing
- For catastrophic and hazardous failure conditions, uses functional failure path analysis



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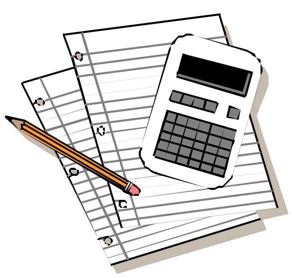
Functional Failure Path (FFP) Analysis (1/10)



- A method of determining the safety critical aspects of an implementation
- A structured, top-down, iterative analysis which identifies functional paths and associated failures

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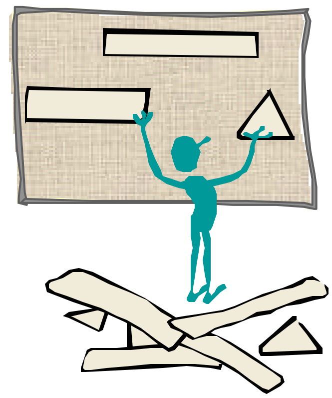
FFP Analysis (2/10)

- Preliminary safety assessment identifies system functional failure paths
- Decompose system functional failure paths



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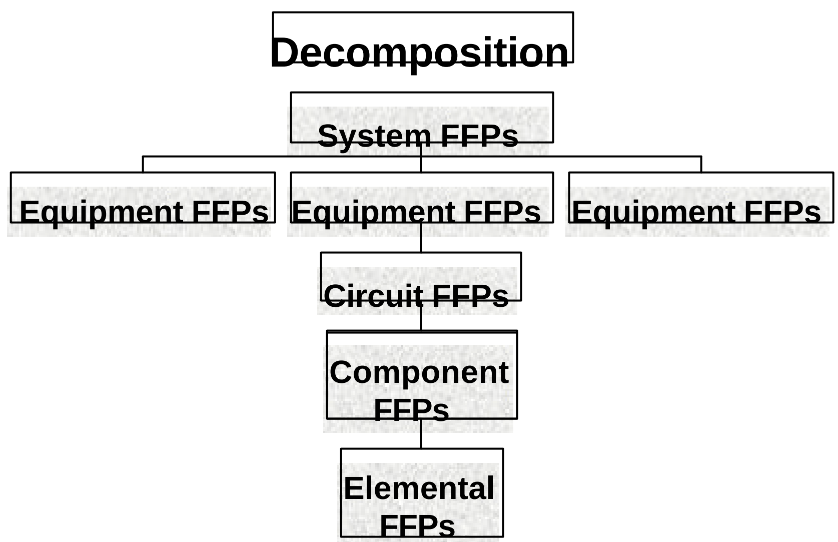
FFP Analysis (3/10)



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FFP Analysis (4/10)

- **FFP analysis method**
  - **Identify functions and required design assurance levels**
  - **Consider means of implementing function and design assurance options**
  - **For FFPs not level A or B, review their relationships to level A and B FFPs**

July 28, 1999 CEH-79

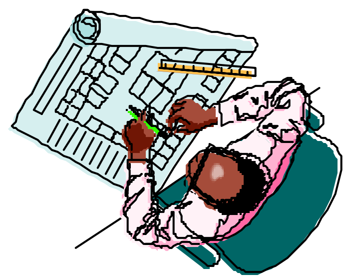
FFP Analysis (5/10)

- **FFP analysis data**
  - **Identify anomalous behavior and/or functional losses**
  - **Identify effects of anomalous behavior and/or functional losses**
  - **Describe relationships between FFPs, independent or interdependent**
  - **Traceability between FFPs and requirements**

July 28, 1999 CEH-80

FFP Analysis (6/10)

- **Design assurance methods**
  - **Architectural mitigation**
    - » **Dissimilar implementation**
    - » **Redundancy**
    - » **Monitors**
    - » **Command/authority limits**



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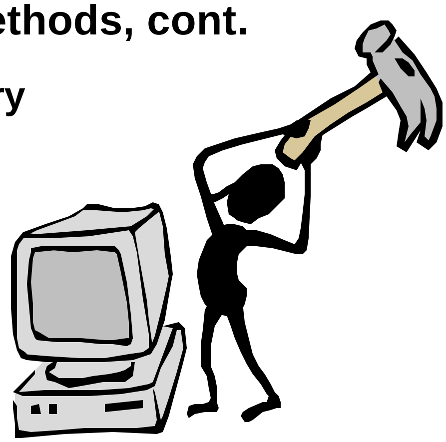
FFP Analysis (7/10)

- **Design assurance methods, cont.**
  - **Product service history**
    - » **Case-by-case basis**
    - » **Engineering judgment**
    - » **Not widely accepted**
    - » **Service history data**



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FFP Analysis (8/10)

- **Design assurance methods, cont.**
  - **Advanced analysis**
    - » **Extends the use of functional failure path analysis**
    - » **FFP analysis is applied progressively at each hierarchical level**
    - » **Three types described - elemental, safety-specific, formal methods**

July 28, 1999 CEH-83

FFP Analysis (9/10)

- **Advanced analysis, cont.**
  - » **Elemental analysis**
    - – **Provide completeness from bottom-up perspective**
    - – **Each element within FFP identified, analyzed, and/or tested**
  - » **Safety-specific**
    - – **In-depth analysis of selected circuit, components**
    - – **Used to derive and validate safety-specific requirements**

July 28, 1999 CEH-84

FFP Analysis (10/10)

- Advanced analysis, cont.
  - » Formal methods
    - – Use of techniques from logic and discrete mathematics
    - – Two broad categories
      - Descriptive - formal specification languages
      - Deductive - explicit enumeration of all assumptions and reasoning steps

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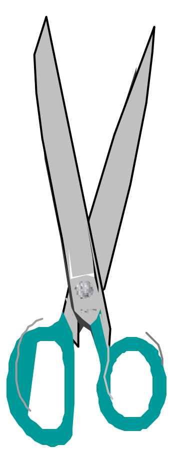
Current Status of Guidelines



- Document too large with too much extraneous text
- Editorial team to spend summer "cleaning up" the document
- Optimistic schedule for completion by end of 1999

July 28, 1999 CEH-86

Summary

- Progress on development assurance guidelines
- Publication early 2000

July 28, 1999 CEH-87

Complex Electronic Hardware

Future FAA Activities

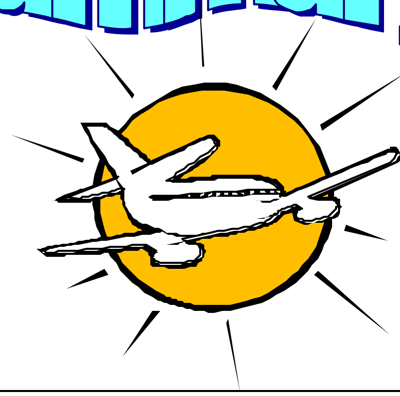
July 28, 1999 CEH-88

C.E.H. Plan

- Release of DO-TBD
- Advisory Circular
- Designee Qualifications
- Research Program
- Training/Case Study

July 28, 1999 CEH-89

Complex Electronic Hardware Summary



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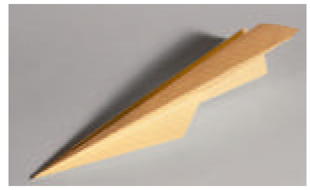
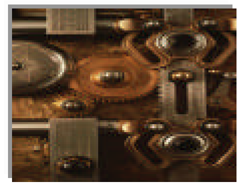
Summary



- PLDs, ASICs, and FPGAs used in aviation



- Complexity leads to safety concerns
- Guidance material being completed
- Policy, guidance, and training being planned

July 28, 1999 CEH-91

Appendix B

Figures for Reference

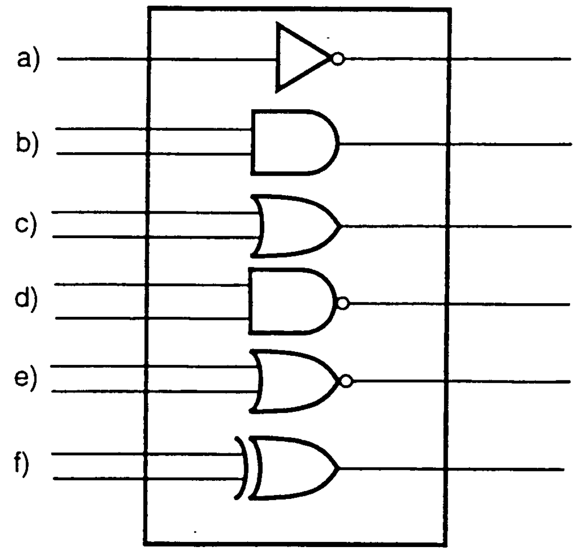


Figure 1: Basic Combinational Logic Elements
(from DOT/FAA/AR-95/31, pg. 8)

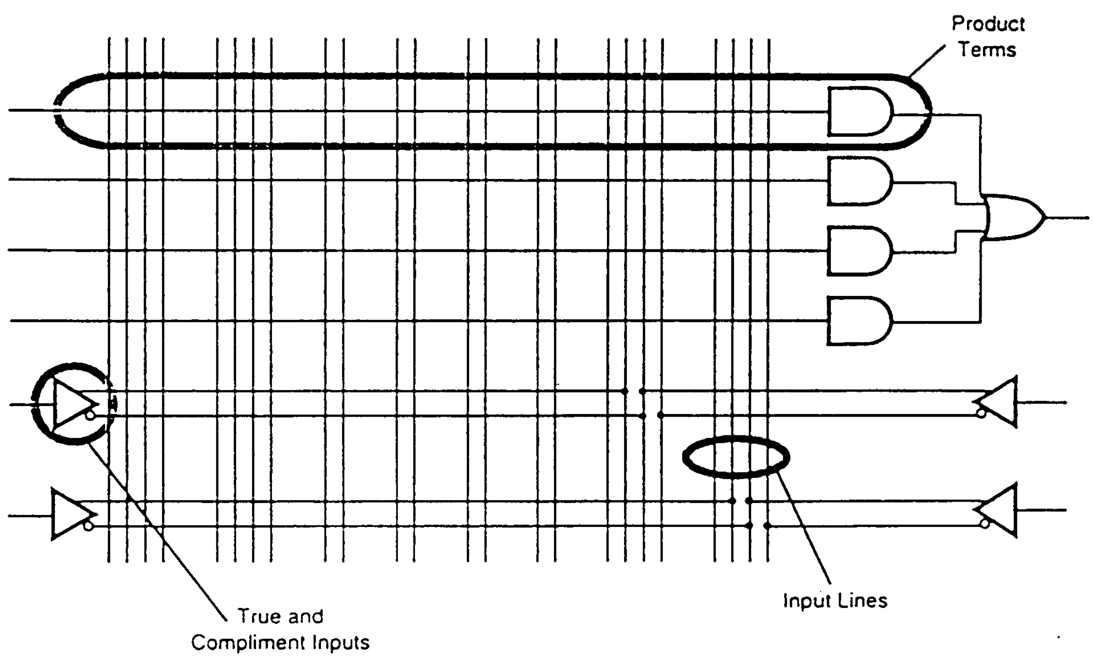


Figure 2: Section of Programmable Array Logic
(from DOT/FAA/AR-95/31, pg. 9)

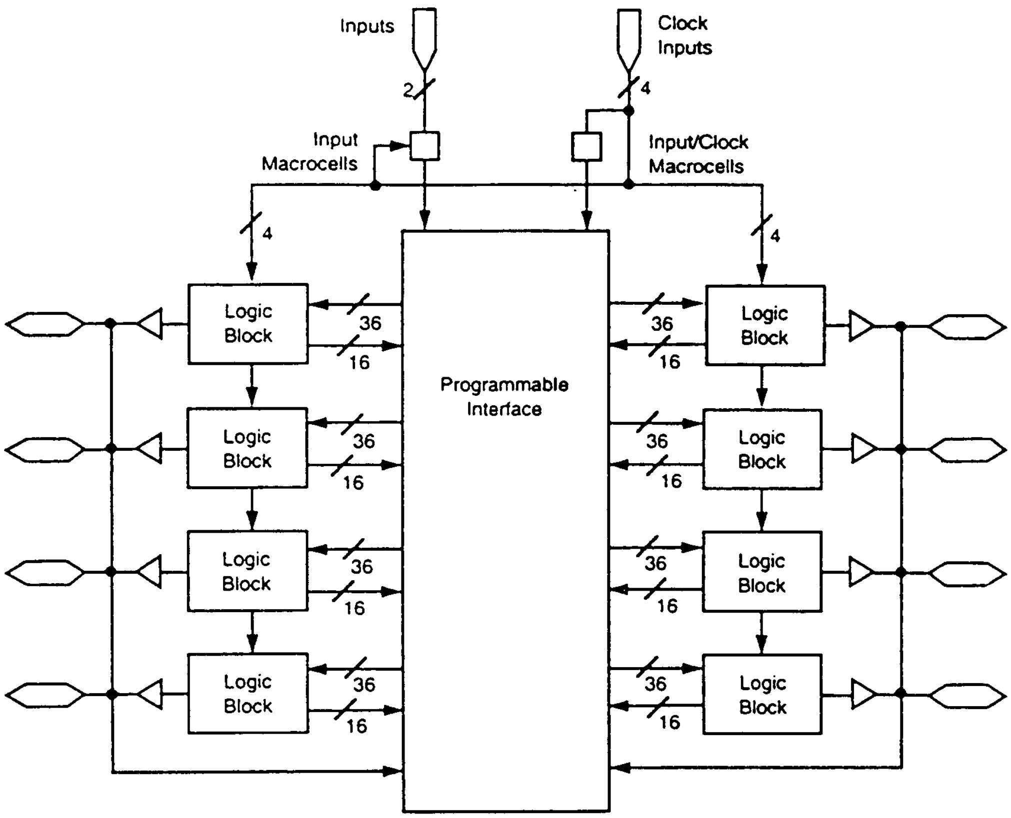


Figure 3: Complex Programmable Logic Device Block Diagram
(from DOT/FAA/AR-95/31, pg. 11)

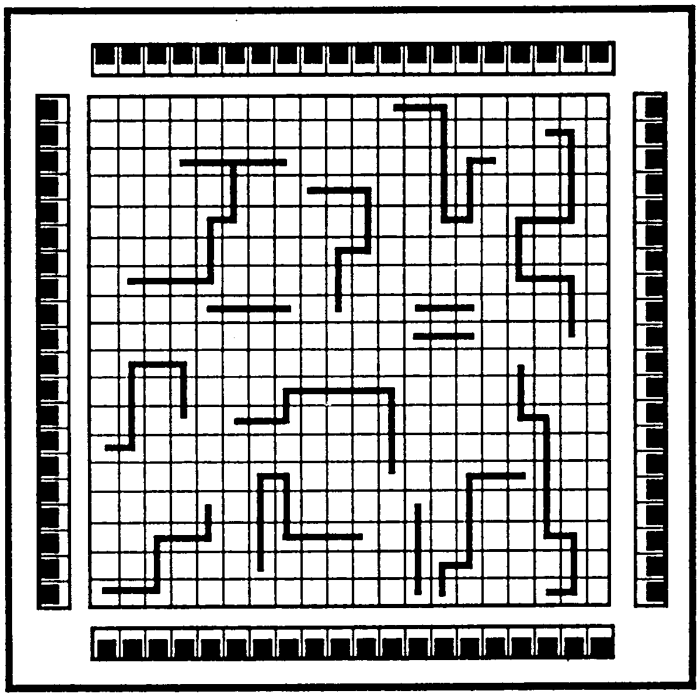


Figure 4: Gate Array Block Diagram
(from DOT/FAA/AR-95/31, pg. 17)

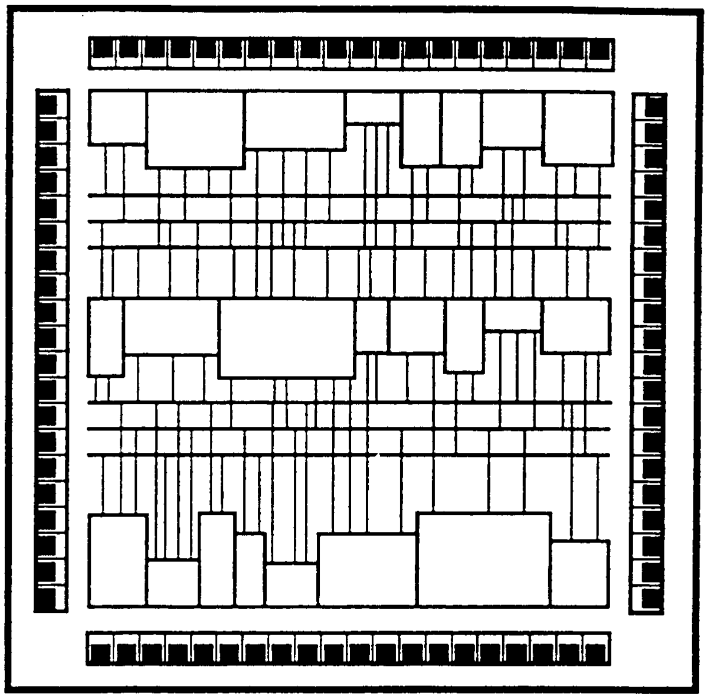


Figure 5: Standard Cell Block Diagram
(from DOT/FAA/AR-95/31, pg. 18)

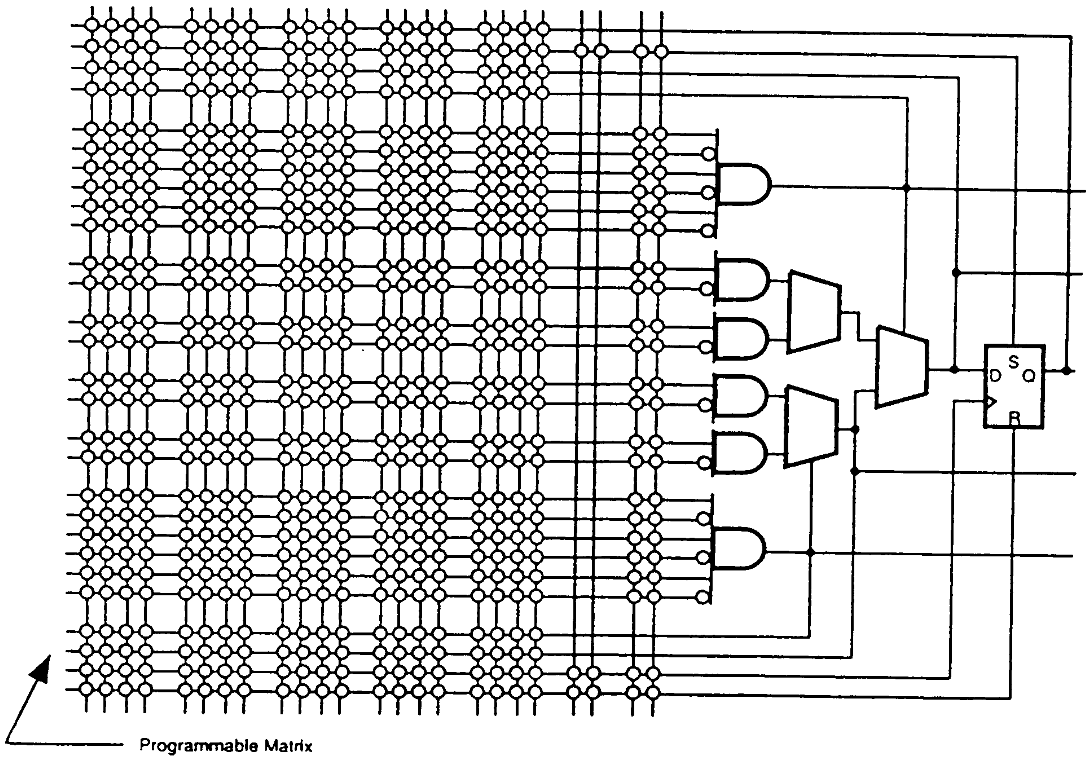


Figure 6: Gate Array Logic Block
(from DOT/FAA/AR-95/31, pg. 21)

Appendix C

Acronym List

AC	Advisory Circular
ACO	Aircraft Certification Office
AHDL	Analog Hardware Description Language
ALU	Arithmetic Logic Unit
ARINC	Aeronautical Radio, Inc.
ASIC	Application Specific Integrated Circuit
ASM	Algorithmic State Machine
ATE	Automatic Test Equipment
ATPG	Automatic Test Pattern Generation
BIST	Built-In Self-Test
BSDL	Boundary Scan Description Language
BSR	Boundary Scan Register
BST	Boundary Scan Test
CAD	Computer Aided Design
CANCER	Computer Analysis of Nonlinear Circuits, Excluding Radiation
CDFG	Control-Data Flow Graph
CE	Certification Engineer
CFI	CAD Framework Initiative
CMOS	Complimentary Metal-Oxide Semiconductor
CPLD	Complex Programmable Logic Device
CPU	Central Processing Unit
CUT	Circuit Under Test
DC	Direct Current
DFG	Data Flow Graph
DFT	Design For Testability
DIP	Dual In-line Package
DMA	Direct Memory Access
DUT	Device Under Test

ECL	Emitter-Coupled Logic
EDA	Electronic Design Automation
EDAC	Error Detection and Correction
EDIF	Electronic Design Interchange Format
EIA	Electronic Industries Association
EPLD	Erasable Programmable Logic Device
EPROM	Erasable Programmable Read-Only Memory
ESD	Electrostatic Discharge
ESDA	Electronic System Design Automation
ESTA	Electronic System Test Automation
FAA	Federal Aviation Administration
FAR	Federal Aviation Regulation
FFB	Fast Function Block
FIPS	Federal Information Processing Standard
FPGA	Field Programmable Gate Array
FSM	Finite State Machine
FSMD	Finite State Machine with Data Path
HCPLD	High Capacity Programmable Logic Device
HDL	Hardware Description Language
HDLC	High-Level Data Link Control
HF	High Frequency
IC	Integrated Circuit
IEC	International Electrotechnical Commission
IEEE	Institute of Electrical and Electronic Engineers
I/O	Input/Output
I_{DD}	CMOS Device dc Power Supply Current
I_{DDQ}	Quiescent State of Power Supply Current IDD
JTAG	Joint Test Action Group

LF	Low Frequency
LFSR	Linear Feedback Shift Register
LIR	Left Instruction Register
LRU	Line Replaceable Unit
LSI	Large Scale Integration
LSSD	Level Sensitive Scan Design
mA	Milliampere
MHz	Megahertz
MOS	Metal-Oxide Semiconductor
MSI	Medium-Scale Integration
MUX	Multiplexer
NAND	Inverting Logical AND Gate
NLFSR	Nonlinear Feedback Shift Register
NMOS	Negative-Well MOS
NOR	Inverting Logical OR Gate
NS	Nanosecond
ORA	Output Response Analyzer
P	Power
PAL	Programmable Array Logic
PC	Personal Computer
PDES	Product Data Exchange Specification
PLD	Programmable Logic Device
PMOS	Positive-Well MOS
PROM	Programmable Read-Only Memory
QTAG	Quality Test Action Group
RAM	Random Access Memory
RC	Resistance-Capacitance
RIR	Right Instruction Register

ROM	Read-Only Memory
RTCA	Requirements and Technical Concepts for Aviation (formerly Radio Technical Commission for Aeronautics)
RTL	Register Transfer Level
SAE	Engineering Society for Advancing Mobility Land Sea Air and Space (formerly Society of Automotive Engineers)
SC-180	Special Committee 180
SC	Scan Control
SCR	Silicon-Controlled Rectifier
SEU	Single Event Upset
SI	Scan In
SO	Scan Out
SPICE	Simulation Program with Integrated Circuit Emphasis
SRAM	Static Random Access Memory
SRC	Scan Register Chain
SSI	Small-Scale Integration
TA	Ambient Temperature
TAP	Test Access Port
Tc	Case (Package) Temperature
TC	Test Clock
TCK	Tester Clock
TDI	Test Data In
TDO	Test Data Out
Tj	Junction Temperature
TMS	Test Mode Select
TPG	Test Pattern Generator
TRST	Test Reset
TTM	Time-To-Market
UIM	Universal Interconnect Matrix

V&V	Verification and Validation
V	Volt
V_{CC}	Collector Supply Voltage
V_{DD}	CMOS Device DC Power Supply Voltage
VHDL	VHSIC Hardware Description Language
VHSIC	Very High Speed Integrated Circuit
VLSI	Very Large Scale Integration

Appendix D

Part 25 Generic Issue Paper

ISSUE PAPER

PROJECT: <COMPANY NAME>
<PRODUCT NAME & MODEL>
<PROJECT NUMBER>

ITEM: S-x

STAGE: 2

REG.REF.: §§ 21.16, 25.1301, 25.1309

DATE:

NATIONAL POLICY REF.: AC 25-1309-1A, AC 20-115B

ISSUE STATUS: OPEN

SUBJECT: Programmed Logic Devices

BRANCH ACTION:

COMPLIANCE TARGET:
Pre-TC/STC/ATC/TSOA

GENERIC ISSUE PAPER

STATEMENT OF ISSUE:
The <COMPANY NAME> <PRODUCT NAME & MODEL> proposes to use Programmed Logic Devices in airborne systems and equipment. At present there is no specific FAA policy or guidance for certification of airborne systems containing Programmed Logic Devices. The purpose of this Issue Paper is to define the specific aspects of certification associated with PLDs for systems containing such devices on the <COMPANY NAME> <PRODUCT NAME & MODEL> program.

BACKGROUND:
Systems used on the <Aircraft Model> will include Programmed Logic Devices. For clarification the following terminology applies:

<u>Programmed Logic Devices</u>
Programmed Logic Devices include Application Specific Integrated Circuits (ASIC) and Programmable Logic Devices (PLDs).

<u>ASIC</u>
An ASIC is defined as any masked programmed integrated circuit that is developed by or for <COMPANY NAME> <Product Name & Model> that requires physical customization of the device die by an ASIC vendor. Gate array, cell based and custom designs are included as they involve some level of customization of the mask sets used in the fabrication of the devices.

PLD

A PLD is defined as any device that is purchased as an electronic part and altered to perform an application specific function. PLDs include, but are not limited to, Programmable Array Logic (PAL) devices, Programmable Logic Array (PLA) devices, General Array Logic (GAL) devices, Field Programmable Gate Array (FPGA) devices, and Erasable Programmable Logic Devices (EPLD). Programmable Logic Devices typically require programming via software which is done in-house by the equipment manufacturer.

These devices will be used in systems which have functions that can affect the safety of the airplane. These devices are often as complex as software controlled microprocessor based systems. Because of the nature and complexity of systems containing digital logic, the FAA has determined that adherence to a structured approach may be used to show compliance with FAR 25.1309 for complex, programmable logic devices. One means of showing such compliance for complex, programmable logic devices is adherence to the guidelines of RTCA document DO-178B, "Software Considerations in Airborne Systems and Equipment", as if these devices were software programs Although systems containing Programmed Logic Devices can perform functions of the same complexity as software based systems, the FAA has no policy or guidelines for certification of systems containing Programmed Logic Devices. However, the problems are essentially the same as for software. This issue paper is concerned with the assurance of the encoded logic embedded in these devices.

FAA POSITION:

There is no existing FAA policy or guidance for showing compliance to the existing rules for those aspects of certification associated with Programmed Logic Devices. Accordingly, certification of systems on the <COMPANY NAME> <PRODUCT NAME & MODEL> which contain such devices will require the following:

Programmed Logic Devices associated with functions whose failure or malfunction could cause or contribute to a catastrophic failure condition for the aircraft as defined in Advisory Circular 25.1309-1A or to a hazardous/severe-major failure condition as defined in RTCA document DO-178B, shall undergo testing which demonstrates correct operation under all combinations and permutations of conditions of the gates within the device, or analysis which can show analogous results.

Programmed Logic Devices associated with functions whose failure or malfunction could cause or contribute to a major or a minor failure condition for the aircraft as defined in Advisory Circular 25-1309-1A shall undergo testing which demonstrates correct operation under all combinations and permutations of conditions at the pins of the device, or analysis which can show analogous results.

In the event that the complexity of the device makes the testing and analysis requirements outlined above unfeasible, the following shall apply:

Programmed Logic Devices shall be developed using a structured development approach approved by the FAA. The structured approach should provide design verification which achieves the same result as that provided for software development by RTCA document DO-178B. The rigor of the structured approach should be commensurate with the hazard associated with failure or malfunction of the system in which the Programmed Logic Device is located. Guidance in this area can be found in the sections of DO-178B which describe the requirements for the software levels associated with software development and assurance. Furthermore, the applicant should ensure that: 1) Programmed Logic Devices are identified in the certification plans, 2) the development approach and rigor of the approach for each device is acceptable to the FAA, and 3) accomplishment summaries describe the means and level of design assurance achieved.

Information on how the applicant intends to present certification data for Programmed Logic Devices can be included in current certification plan documents or as stand-alone plans for Programmed Logic Devices.

Requirements identified in this issue paper do not in any way alleviate the need for traditional methods for hardware design and assurance.

FCAA POSITION:

APPLICANT POSITION:

CONCLUSION:

Manager, Transport Airplane Directorate
Airplane Certification

Date

Appendix E

Informative Articles

The following articles from *EDN* Magazine provide additional insight into Complex Electronic Hardware.

Field-programmable Devices,
October 10, 1996 issue, pages 201-206.

HDL basic training: top-down chip design using Verilog and VHDL,
October 24, 1996 issue, pages 103-112.

***VHDL and Verilog fundamentals -
design entities, data types, and data objects***,
February 3, 1997 issue, pages 163-168.

***VHDL and Verilog fundamentals -
expressions, operands, and operators***,
April 10, 1997 issue, pages 207-214.

For more information, see ***www.ednmag.com***.

Appendix F

Course Evaluation Forms

There are two course evaluation forms in this appendix. Please select the one appropriate for your course of study.

- IVT broadcast
- Self-study video course

If you are taking this course via IVT and you are logged on to a keypad, you will be asked to complete the course evaluation by using the Viewer Response System Keypad. Your IVT instructor will provide directions on how to complete the course evaluation. If you do not have access to a keypad, circle your responses and fax the form to the IVT studio (405-954-0317 / 9507).

If you have completed this by watching the video, please complete the Self-Study Evaluation Form and return it to your directorate/division training manager (ATM).

IVT COURSE EVALUATION
AIR – Complex Electronic Hardware
July 28, 1999

Please give us your candid opinions concerning the training you've just completed. Your evaluation of the IVT course is important to us, and will help us provide the best possible products and services to you. **NOTE: Your keypad responses are not identifiable by name; only averages of the item responses are provided to the instructor and to others responsible for the training.**

Use your Viewer Response Keypad to answer the following questions.

	Very Good	Good	Average	Poor	Very Poor
1. Length of course	A	B	C	D	E
2. Depth of information	A	B	C	D	E
3. Pace of training	A	B	C	D	E
4. Clarity of objectives	A	B	C	D	E
5. Sequence of content	A	B	C	D	E
6. Quality of course materials	A	B	C	D	E
7. Quality of graphics/visual aids	A	B	C	D	E
8. Readability of text on monitor	A	B	C	D	E

		Very Good	Good	Average	Poor	Very Poor
9.	Effectiveness of instructor(s)	A	B	C	D	E
10.	Communication between student and instructor	A	B	C	D	E
11.	Applicability of material to your job.	A	B	C	D	E
12.	Overall quality of the course	A	B	C	D	E
13.	Overall effectiveness of the IVT format	A	B	C	D	E

14. Would you like to take other IVT courses?

A. YES **B.** NO **C.** UNDECIDED

15. On the key pad, enter your number of years of FAA experience.

________ (***number/enter***)

When finished, press the "Next Quest" key on your keypad and answer YES, then Enter. Your responses will be sent electronically. Individual responses are not tabulated; only item averages for each question are presented to the instructor(s) and to AIR-510.

Additional Comments may be faxed to the IVT Studio:

405-954-0317 / 9507

Self-Study Video Course Evaluation
AIR – Complex Electronic Hardware
Original Broadcast Date: July 28, 1999

Please give us your candid opinions concerning the training you've just completed. Your evaluation of the self-study video course is important to us, and will help us provide the best possible products and services to you.

Course Title: ____

Date: ______________________

Number of years of FAA experience: _____________

(Optional)

Name: Office phone: ( )

For the following, please completely darken the circle appropriate to your response.

	Very Good	Good	Average	Poor	Very Poor	N/A
1. Length of course	○	○	○	○	○	○
2. Depth of information	○	○	○	○	○	○
3. Pace of training	○	○	○	○	○	○
4. Clarity of objectives	○	○	○	○	○	○
5. Sequence of content	○	○	○	○	○	○
6. Amount of activities/practice	○	○	○	○	○	○
7. Quality of course materials	○	○	○	○	○	○
8. Effectiveness of instructor(s)	○	○	○	○	○	○
9. Overall quality of the course	○	○	○	○	○	○
10. Overall effectiveness of the self-study video format	○	○	○	○	○	○

11. Rate your level of knowledge of the topic before and after taking this self-study course.

	Very Low	Low	Moderate	High	Very High
BEFORE THE COURSE:	O	O	O	O	O
AFTER THE COURSE:	O	O	O	O	O

12. What did you like best about the course?

13. What would you improve in the course?

14. What previous experience, if any, have you had with self-study courses?

O None O Moderate O Considerable

15. Were you comfortable with the self-study video format?

O Yes O No O Undecided

If not, why not?

16. Would you like to take other self-study video courses?

O Yes O No O Undecided

If not, why not?

17. Additional comments:

PLEASE SEND THIS COMPLETED FORM TO YOUR DIRECTORATE/DIVISION TRAINING MANAGER (ATM). THANK YOU.